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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,527	03/24/2006	Kiyoshi Kato	0756-7660	5487

31780 7590 05/28/2009

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EXAMINER	
WOLDEGEORGIS, ERMIAS T	

ART UNIT	PAPER NUMBER
2893	

MAIL DATE	DELIVERY MODE
05/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,527	KATO ET AL.	
	Examiner	Art Unit	
	ERMIAS WOLDEGEORGIS	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/02/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. ***Response to Amendment***

Claims 1-16 are currently pending.

2. ***Priority***

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

3. ***Information Disclosure Statement***

The information disclosure statement (IDS) filed on 2/02/2009 has been acknowledged and a signed copy of the PTO-1449 is attached herein.

4. ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Koyama et al. **(PG PUB No. US. 2005/0174845 A1, hereinafter "Koyama")**.

In regards to claim 1, Koyama discloses (Figure 15) a memory device comprising a memory cell **(memory element (N-type TFT))** formed over an insulating surface **(3000)**, which includes a semiconductor film **(3003)** having two impurity regions **(3014/3015, Par [0120])**, a gate electrode **(3007/3011)**, and two wirings **(3026/3027)** connected to the respective impurity regions **(3014/3015, Par [0120])**, wherein the semiconductor film **(3003)** interposed between the two wirings **(3026/3027)** of the memory cell **(memory element (N-type TFT))** is altered **(characteristics of the polysilicon and polycrystalline SiGe, Par [0113])** by applying a voltage **(Par [0085] and for the proper function of the device)** between the gate electrode **(3007/3011)** and at least one of the two wirings **(3026/3027)**.

In regards to claim 2, Koyama discloses (Figure 15) the memory device **(memory element (N-type TFT)** comprises two or more gate electrodes **(3007/3011)**.

In regards to claim 3, Koyama discloses (Figure 15) the semiconductor film **(3003)** is altered to an insulating state by applying a voltage **(Par [0085])** between the gate electrode **(3007/3011)** and at least one of the two wirings **(3026/3027)**.

In regards to claim 4, Koyama discloses (Figures 22A-23I) a memory device comprising a first memory cell **(71)** and a second memory cell **(72)** formed over an insulating surface **(60/61)**, each of which includes a semiconductor film **(57)** having two impurity regions **(65/68)**, a gate electrode **(56)**, and two wirings **(51)** connected to the respective impurity regions **(65/68)**, wherein the first memory cell **(71)** comprises an initial state **(this is inherently there at least**

one bit to tell whether data is stored or not); and the semiconductor film **(57)** interposed between the two wirings **(51)** of the second memory cell **(72)** is altered by applying a voltage **(Par [0085])** between the gate electrode **(56)** and at least one of the two wirings **(51)**.

In regards to claim 5, Koyama discloses (Figure 15) the memory device **(memory element (N-type TFT))** comprises two or more gate electrodes **(3007/3011)**.

In regards to claim 6, Koyama discloses (Figure 15) the semiconductor film **(3003)** is altered to an insulating state by applying a voltage **(Par [0085])** between the gate electrode **(3007/3011)** and at least one of the two wirings **(3026/3027)**.

In regards to claim 7, Koyama discloses (Figure 15) a memory device comprising a memory cell **(memory element (N-type TFT)** formed over an insulating surface **(3000)**, which includes a semiconductor film **(3003)** having one or two impurity regions **(3014/3015)**, an electrode **(3007/3011)**, and two wirings **(3026/3027)** connected to the respective impurity regions **(3014/3015)**,wherein the semiconductor film **(3003)** interposed between the two wirings **(3026/3027)** of the memory cell **(memory element (N-type TFT))** is altered by applying a voltage **(Par [0019])** between the electrode **(3007/3011)** and at least one of the two wirings **(3026/3027)**.

In regards to claim 8, Koyama discloses (Figure 15) the electrode **(3007/3011)** is interposed between the two wirings **(3026/3027)**.

n regards to claim 9, Koyama discloses (Figure 15) the memory device **(memory element (N-type TFT))** comprises two or more electrodes **(3007/3011)**.

In regards to claim 10, Koyama discloses (Figure 15) the semiconductor film **(3003)** is altered to an insulating state by applying a voltage **(Par [0019])** between the gate electrode **(3007/3011)** and at least one of the two wirings **(3026/3027)**.

In regards to claim 11, Koyama discloses (Figure 22A-23I) a memory device comprising a first memory cell **(71)** and a second memory cell **(72)** formed over an insulating surface **(60/61)**, each of which includes a semiconductor film **(57)**having one or two impurity regions **(65/68)**, an electrode **(56)**, and two wirings **(51)** connected to the respective impurity regions **(65/68)**, where in the first memory cell **(71)** has an initial state **(this is inherently there at least one bit to tell whether data is stored or not)**; and the semiconductor film **(57)** interposed between the two wirings **(51)** of the second memory cell **(72)** is altered by applying a voltage **(Par [0085])** between the electrode **(56)** and at least one of the two wirings **(51)**.

In regards to claim 12, Koyama discloses (Figures 22A-23I) the electrode **(56)** is interposed between the two wirings **(51)**.

In regards to claim 13, Koyama discloses (Figures 22A-23I) the memory device **(memory 74)** comprises two or more electrodes **(56)**.

In regards to claim 14, Koyama discloses (Figures 22A-23I) the semiconductor film **(57)** is altered to an insulating state by applying a voltage **(Par [0019])** between the gate electrode **(56)** and at least one of the two wirings **(51)**.

In regards to claim 15, Koyama discloses (Figures 22A-23I) a manufacturing method of a memory device, comprising the steps of: forming an island shape semiconductor film **(Par [0160])** over an insulating surface **(60/61)**; forming a gate insulating film **(Par [0168])** over the island shape semiconductor film **(57)**; forming a gate electrode **(Par [0169])** over the gate insulating film **(58)**; doping an N-type impurity element **(Par [0120] and Par [0180])** with the gate electrode used as a mask **(an N-type impurity element 78 (typically P or As) is doped at a high concentration with the gate electrode 56 and the sidewall 76 used as a mask Par [0180])**, thereby forming an N-type high concentration impurity region **(78)** in the island shape semiconductor film **(57)**; forming an interlayer film **(Par [0153])** over the gate insulating film **(58)** and the gate electrode **(56)**; forming a contact hole **(Par [0185])** in the interlayer film **(53)** and a wiring **(51)** connected to the high concentration impurity region **(78)**, thereby forming a memory cell **(memory 74)**, and applying a voltage between the gate electrode and the wiring of the memory cell, thereby altering a channel region of the island shape semiconductor film to an insulating state **(Par [0085])**.

In regards to claim 16, Koyama discloses (Figures 22A-23I) the memory device **(memory 74)** comprises two or more gate electrodes **(56)**.

6. ***Response to Arguments***

Applicant's arguments filed 2/06/2009 have been fully considered but they are not persuasive.

Applicant makes the following argument:

1. Paragraphs [0019] and [0085] of Koyama, while generally referring to blowing a fuse element, do not appear to specifically disclose that a semiconductor film interposed between two wrings of a memory cell is altered by applying a voltage between a gate electrode and at least one of two wirings.

This is not persuasive because Par [0085] of Koyama teaches or suggests that there is heat generation during the operation of the device and Koyama in Par [0113] teaches that the semiconductor layer 3003 is formed from silicon or silicon-germanium. It is also clear that the operation of the device needs application of voltage on the gate electrode and on one of the other wirings (creating potential difference between source and drain) for current to flow. Examiner believes that as the current flows through the semiconductor layer 3003, a heating takes place which alters the semiconductor layer. For example, see US 2007/0034608 A1 Par [0004], which asserts that it is known that certain thermally-mutable materials, such as polycrystalline (polysilicon) or polycrystalline SiGe, respond to heating or voltage pulses by changing their electrical resistivity. Therefore, as the device operates and due to heat generation and/or voltage pulses the alteration of the semiconductor layer will be taking place.

2. "The Official Action asserts that the first impurity region 3014 and 3015 in Koyama correspond with "two impurity regions" in the rejection of claim 1 (page 3, Paper No. 20080916)

and as "one or two impurity regions" in the rejection of claim 7 (page 4, Id.). Similarly, the Official Action asserts that the low concentration impurity regions 65 and the high concentration impurity regions 68 correspond with "two impurity regions" in the rejection of claim 4 (page 3, Id.) and as "one or two impurity regions" in the rejection of claim 11 (page 5, Id.). These assertions appear to be contradictory, and the Applicant respectfully submits that Koyama fails to teach both one and two impurity regions as presently claimed." (Remarks Page 3 Par 2)

This is not persuasive because claims 1, 4, 7 and 11 are all independent claims and were rejected with different embodiments of the prior art. For example, claims 1 and 7 were rejected using embodiment 5 whereas claims 4 and 11 were rejected using embodiment 10. So there are no contradictory assertions in rejecting these claims because all of these four claims stand independently of the others and rejected with various variations of the prior art. Furthermore, rejections by the same embodiments of the Koyama art were not shown to be inconsistent.

7. ***Conclusion***

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERMIAS WOLDEGEORGIS whose telephone number is (571)270-5350. The examiner can normally be reached on Monday through Friday 8:30 AM to 6:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daveinne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ERMIAS WOLDEGEORGIS/

Examiner, Art Unit 2893

/A. Sefer/
Primary Examiner
Art Unit 2893